

SESSION 9b: DEVICE TECHNOLOGY

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The device technology session has four regular papers and one student paper, all having practical and relevant information for device engineers. The first paper, from WIN semiconductor, discusses how to compensate for natural variations in an epitaxial layer structure through utilizing gate metal sinking in an E/D mode pHEMT process and thus achieve better consistency of pinchoff voltage of the EFETs. The second paper, also from WIN, details a 0.1 um pHEMT foundry process on 6" wafer for V band applications. The process features I_{max} of 720 mA/mm, V_p of -0.9 V, f_T of 135 GHz, P_{max} of 850 mW/mm at $V_{dd}=4$ V, gain of 8-9 dB at 70-90 GHz, and F_{min} of 0.8 dB at 40 GHz. The third paper, from Hitachi Cable, shows the methodology used to optimize buffer layer structure of high power MESFETs used in power amplifiers. The fourth paper, from Avago Technologies, details the optimization of Boron isolation implant doses and energies for a GaAs HBT device so that low junction leakage and high isolation resistance are achieved simultaneously. The last paper is a student paper from Georgia Tech. It shows exciting device results for a GaN HBT process. Collector current density of 19.8 kA/cm² is achieved with a BV_{ceo} of 110V and knee voltage of $< 2.1V$.