

GaN/InGaN Heterojunction Bipolar Transistors with Collector Current Density > 20 kA/cm²

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Abstract -- We report GaN/In_{0.03}Ga_{0.97}N *npn* heterojunction bipolar transistors (HBTs) grown on sapphire substrates by metalorganic chemical vapor deposition (MOCVD). The common-emitter *I-V* characteristics show a collector current density (J_C) > 20 kA/cm² with a low collector offset voltage (V_{offset}) of 0.22 V and a knee voltage (V_{knee}) of 2.1 V. The maximal small-signal differential current gain (h_{fe}) of 38 and J_C of > 28.6 kA/cm² are also measured. The measured BV_{CEO} is 110 V. The cut-off frequency (f_T) of 3.0 GHz is also measured at $J_C = 11.8$ kA/cm².

INTRODUCTION

III-Nitride (III-N) transistor technologies have been actively developed for more than ten years as promising new choices for high-power RF amplification. Thanks to the wide bandgap (WBG) and high electron saturation velocity properties, III-N transistors combine the advantages of high-power handling capability and high-frequency operation for next-generation RF technologies. The WBG III-N semiconductors are also a suitable material system for high-temperature electronics. Therefore, III-N RF transistor technologies are attracting great interests for high-performance circuits and subsystems that enable compact chip size with high output power density in commercial and military applications.

The III-N transistor technologies mainly include III-N heterojunction bipolar transistors (HBTs) and III-N heterojunction field effect transistors (HFETs). III-N RF HFETs have been extensively studied and commercialized for over a decade. On the other hand, however, the progress on III-N HBT development has been slow. When compared to HFETs, HBTs are preferred for linear power amplifiers because of the higher power density, linear current gain, and uniform device turn-on characteristics. However, a number of obstacles inhibit the development of III-N HBTs. For III-N *npn* HBTs, the major issue is the low-conductivity base layer, resulting from the difficulty of achieving high free-hole concentration and the inevitable plasma-induced dry-etching damage and the consequent type-conversion. Most

of the III-N *npn* HBTs developed in earlier dates had to employ a complex re-growth schemes to achieve functional transistor actions [1, 2].

Recent progresses on the much refined MOCVD epitaxial material growth and device fabrication techniques have enabled several GaN/InGaN *npn* HBT demonstrations that used a single-pass epitaxial growth scheme [3-10]. These results showed that good d.c. performance can be realized on III-N HBTs without the need for additional re-growth schemes. To further develop a viable III-N HBT technology for RF power amplification, high J_C , low V_{offset} and low V_{knee} are highly desired. In this study, we present a GaN/InGaN *npn* HBT fabrication process that can achieve low-resistive metallization contacts and low-damage etched sidewall surface that lead to dramatic d.c. performance enhancement in GaN/InGaN HBTs. The common-emitter *I-V* characteristics show that a collector current density (J_C) > 20 kA/cm² with a low collector offset voltage (V_{offset}) of 0.22 V and a knee voltage (V_{knee}) of 2.1 V can be achieved on these HBTs. We also demonstrate the first GaN/InGaN HBTs with f_T of > 3.0 GHz in this paper.

DEVICE STRUCTURE AND FABRICATION

The epitaxial GaN/InGaN *npn* HBT structure is grown on a 2-inch *c*-plane sapphire substrate in a Thomas-Swan MOCVD system. The detailed material growth development was reported earlier [11]. Table I shows the epitaxial layer structure used in this study. The epi-layer growth starts with a 2500-nm unintentionally-doped (UID) GaN buffer layer, followed by a 1000-nm highly Si-doped n^+ -GaN sub-collector and a 500-nm lightly Si-doped n -GaN collector. The free-electron concentration is 3×10^{18} cm⁻³ for the sub-collector and 1×10^{17} cm⁻³ for the collector. Between the base and collector, a 30-nm n -In_xGa_{1-x}N ($x = 0 \sim 0.03$) collector grading layer is included to mitigate the conduction band discontinuity at the base-collector junction. The base is a 100-nm Mg-doped p -In_{0.03}Ga_{0.97}N layer with the free-hole concentration of 1×10^{18} cm⁻³. A 30-nm n -In_xGa_{1-x}N ($x = 0.03 \sim 0$) emitter grading layer is included in between the base and the emitter to accommodate the strain induced at

the base-emitter junction. Finally, a 70-nm highly-doped n^+ -GaN emitter layer with the free-electron concentration of $1 \times 10^{19} \text{ cm}^{-3}$ is grown to complete the HBT growth.

TABLE I: THE LAYER STRUCTURE OF $n\text{p}n$ GaN/INGaN HBTs

Layers	Material	Thick-ness (nm)	Dop-ant	Free-carrier Conc. (cm^{-3})
Emitter	GaN	70	Si	1×10^{19}
Emitter grading	GaN to $\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$	30	Si	1×10^{19}
Base	$\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$	100	Mg	1×10^{18}
Collector grading	$\text{In}_{0.03}\text{Ga}_{0.97}\text{N}$ to GaN	30	Si	1×10^{18}
Collector	GaN	500	Si	1×10^{17}
Sub-collector	GaN	1000	Si	3×10^{18}
Buffer	GaN	2500		UID

The fabrication processing flow is compatible with conventional GaAs-based HBT fabrication procedures. A i -line contact aligner is used for the photolithography steps. A Cl_2 -based inductively coupled plasma etching system is employed for the emitter mesa, base mesa and the device isolation steps. An ultraviolet-enhanced electrode-less wet-etching surface treatment is also applied to remove post-dry-etching-induced surface damages [12]. Ti/Al-based metal stacks are deposited to form the ohmic contact on the n -type emitter and sub-collector layers. The specific contact resistances of the emitter and the sub-collector are $< 2 \times 10^{-6} \Omega\text{-cm}^2$. The sheet resistance of the emitter and sub-collector are $1150 \Omega/\square$ and $85 \Omega/\square$, respectively. The p -type InGaN base contact uses a Ni/Au metal stack. However, the base contact is slightly Schottky due to the relatively low free-hole concentration and the dry-etching-induced type-conversion on the external base surface. The post-device processing steps include the Benzocyclobutene (BCB) passivation and via hole opening dry etching. The on-wafer NiCr resistor is also deposited. Finally, a thick Ti/Au layer is evaporated to form the probing pads. Fig. 1 shows an SEM picture of a $4 \times 10 \mu\text{m}^2$ HBT prior to the post-device processing steps.

D.C. CHARACTERISTICS

Fig. 2 shows a set of common-emitter I - V family curves of a GaN/InGaN HBT with the emitter area (A_E) = $3 \times 3 \mu\text{m}^2$. The base current (I_B) increases from $5 \mu\text{A}$ to $70 \mu\text{A}$ with an increment of $5 \mu\text{A}/\text{step}$. The collector voltage (V_{CE}) is swept from 0 to 5 V. At $I_B = 70 \mu\text{A}$, J_C reaches $19.8 \text{ kA}/\text{cm}^2$ ($I_C = 1.78 \text{ mA}$) with a d.c. current gain β ($\equiv I_C/I_B$) of 25. It is also shown that V_{offset} is 0.22 V and V_{knee} is 2.1 V at $J_C = 19.8 \text{ kA}/\text{cm}^2$. At higher V_{CE} , J_C decreases due to the self-heating effect. Fig. 3 shows that the BV_{CEO} is 110 V with a low off-state leakage of 7 nA near the device breakdown.

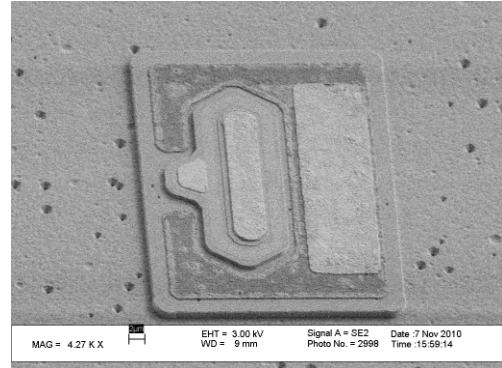


Fig. 1. A SEM picture of a HBT ($A_E = 4 \times 10 \mu\text{m}^2$) prior to the device passivation.

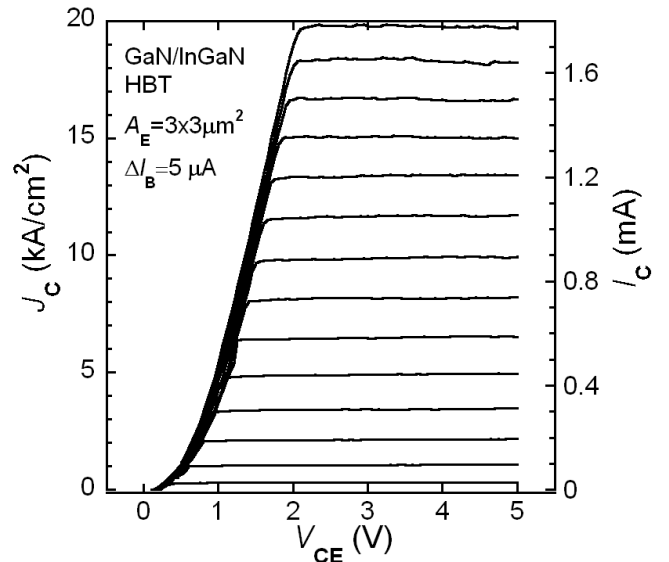


Fig. 2. Common-emitter I - V family curves of a GaN/InGaN HBT ($A_E = 3 \times 3 \mu\text{m}^2$).

Fig. 4 is a Gummel plot of the same HBT device at $V_{CB} = 0 \text{ V}$. At $V_{BE} = 9.5 \text{ V}$, a maximal h_{fe} ($\equiv \Delta I_C / \Delta I_B$) of 38 and I_C of 1.75 mA ($J_C = 19.4 \text{ kA}/\text{cm}^2$) is achieved. At $V_{BE} = 10 \text{ V}$, I_C reaches 2.58 mA with a corresponding J_C as high as $28.6 \text{ kA}/\text{cm}^2$. The Gummel plot measurement is consistent with the common-emitter family curves, indicating normal base-collector junction behavior in these transistors.

It is noted that the V_{BE} in the Gummel plot is much larger than that for a typical III-V HBT. From the I_B vs. V_{BE} data in the Gummel plot, the base-emitter diode series resistance (R_{BE}) is about $22.7 \text{ k}\Omega$. Since the emitter resistance (R_E) is approximately 24Ω , the base resistance (R_B) is estimated to be $22 \text{ k}\Omega$, which dominates the series resistance component at the BE junction. Consequently, the relatively large V_{BE} is mainly attributed to the high R_B value.

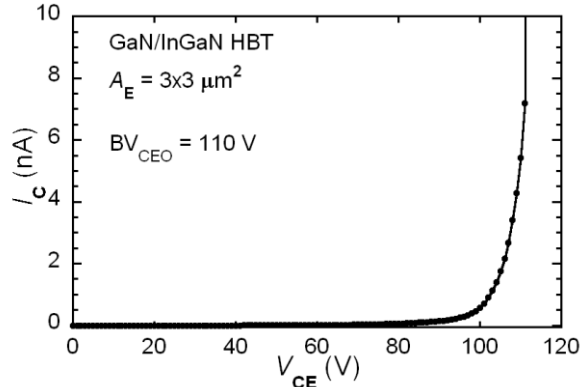


Fig. 3. The BV_{CEO} measurement on a GaN/InGaN HBT ($A_E = 3 \times 3 \mu\text{m}^2$).

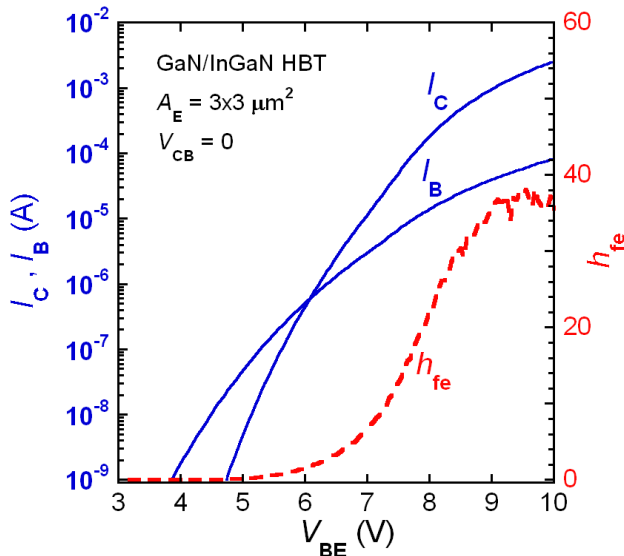


Fig. 4. The measured Gummel plot of a GaN/InGaN HBT ($A_E = 3 \times 3 \mu\text{m}^2$).

RF CHARACTERISTICS

The small-signal S-parameters of GaN/InGaN *npn* HBTs are measured using an Anritsu 37397D Vector Network Analyzer from 40 MHz to 10 GHz at room temperature. On-wafer SOLT calibrations are used for the device characterization. As shown in Fig. 5, the $|h_{21}|^2$ and MAG/MSG of an HBT with $A_E = 3 \times 5 \mu\text{m}^2$ are measured at $V_{CE} = 6 \text{ V}$ and $J_C = 11.8 \text{ kA/cm}^2$. A 20 dB/decade roll-off approximation is used to interpolate the $|h_{21}|^2$ curve at 0dB and the resulting f_T of 3.0 GHz is obtained. To the best of our knowledge, this is the first demonstration of GaN/InGaN HBTs with $f_T > 3.0 \text{ GHz}$. The small-signal modeling indicates that the high-frequency tailing of the $|h_{21}|^2$ curve is mainly due to the capacitive coupling between the emitter metal pad and the slightly *n*-doped UID GaN buffer layer. The measured f_{max} is 950 MHz at MAG/MSG = 0 dB. The fact that f_{max} is lower than f_T indicates that large R_B is still a challenge to achieve higher power gain.

As shown in Fig. 6, the f_T and f_{max} are plotted versus different J_C on the same HBT under test. This issue may

result from the poor heat conductivity and/or the high dislocation density for GaN-based HBTs grown on the sapphire substrate. It can be expected that a better f_T and f_{max} performance could be achieved for III-N HBTs grown on substrates with good thermal conductivity and low defect density.

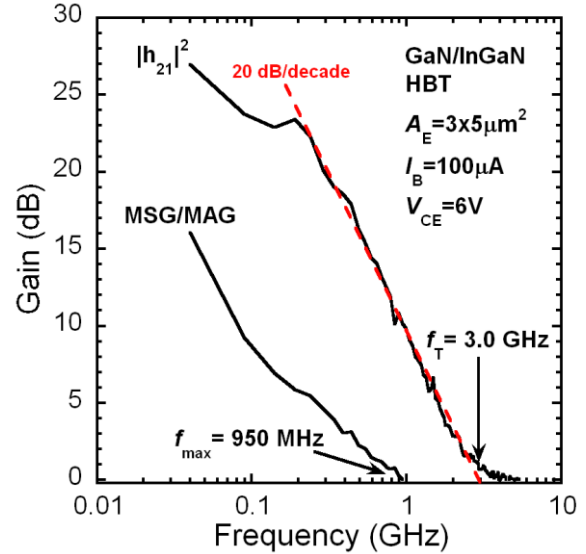


Fig. 5. The measured $|h_{21}|^2$ and MAG/MSG of a $3 \times 5 \mu\text{m}^2$ GaN/InGaN HBT.

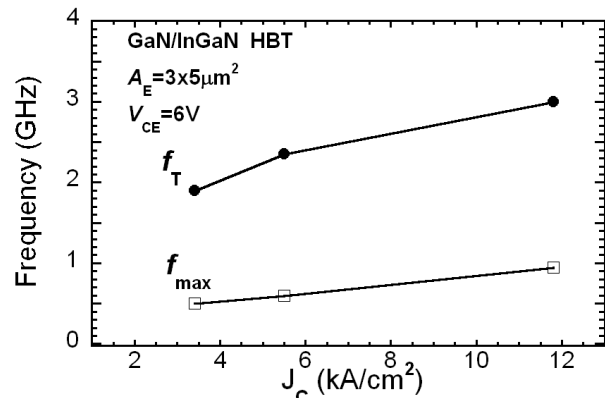


Fig. 6. The f_T and f_{max} of a $3 \times 5 \mu\text{m}^2$ GaN/InGaN HBT at different J_C .

CONCLUSIONS

In summary, we report GaN/In_{0.03}Ga_{0.97}N *npn* HBTs grown on sapphire substrates that can achieve high J_C , high breakdown voltage, low V_{offset} , and low V_{knee} characteristic. The common-emitter measurement results show $J_C > 20 \text{ kA/cm}^2$ with V_{offset} of 0.22 V and V_{knee} of 2.1 V. The BV_{CEO} is 110 V with low off-state leakage. Maximal h_{fe} of 38 is also measured in the Gummel plot at $V_{CB} = 0 \text{ V}$. These values are among the best d.c. characteristics reported to date for III-N HBTs. It is also the first demonstration of GaN/InGaN HBT that can achieve f_T of $> 3.0 \text{ GHz}$.

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ACRONYMS

III-N: III-Nitride
HBT: Heterojunction Bipolar Transistor
HEMT: High-Electron Mobility Transistor
LDMOS: Laterally Diffused Metal Oxide Semiconductor
pHEMT: pseudomorphic HEMT
MOCVD: MetalOrganic Chemical Vapor Deposition
 J_C : Collector current density
 V_{offset} : Offset voltage
 V_{knee} : Knee voltage
 f_T : Short circuit unit-gain frequency
 f_{max} : Maximum oscillation frequency
 h_{fe} : Differential current gain
BCB: Benzocyclobutene