

Cavity structure GaAs FETs with high humidity resistance

Yasuki Aihara¹, Toshiaki Kitano¹, Kazuyo Endo², Kenji Hosogi¹, Hiroshi Fukumoto²

¹High Frequency & Optical Device Works, Mitsubishi Electric Corporation,
4-1, Mizuhara, Itami, Hyogo, 664-8641, Japan

²Advanced Technology R&D Center, Mitsubishi Electric Corporation,
8-1-1 Tsukaguchi-honmachi, Amagasaki, Hyogo, 661-8661, Japan
E-mail Aihara.Yasuki@ab.MitsubishiElectric.co.jp

Keywords: Cavity, humidity resistance, HAST, SAM

Abstract

We have developed new cavity structure GaAs FETs with high humidity resistance. The cavity is formed by sealing up with air bridges and polymers around the FETs and covering the surface of the polymers with thick SiN films. As the cavities formed by the newly-developed process are completely air-filled, the high frequency characteristics of FETs are unaffected by the parasitic capacitances of the polymer films and the thick SiN films. Highly reliable DC operation of the cavity FETs is demonstrated for more than 96 hrs under $T_a = 130^\circ\text{C}$, $\text{RH} = 85\%$ and $V_{dg} = 11\text{ V}$.

INTRODUCTION

High humidity resistant GaAs FETs using non-hermetic packages have been required to produce low-cost high frequency devices in recent years. Various methods have been examined to improve the humidity resistance of the GaAs FETs used in non-hermetic packages. Although passivations of FETs by thick SiN films are effective in improving the resistance, the increases in the parasitic capacitance of the films deteriorate the high frequency characteristics of FETs. A surface treatment¹ prior to deposition of an SiN film can effectively suppress the corrosion reaction between the H_2O and the semiconductor surface of the FETs. However, the surface treatment needs precise control in order to maintain reproducibility. On the other hand, the wafer level package (WLP)² has been actively developed as a promising method of satisfying both high humidity resistance and low parasitic capacitance. However, we consider that it might not be necessarily the best solution from the viewpoint of costs. In this work, we developed new cavity structure FETs with high humidity resistance to be able to pursue both low cost and high productivity. We demonstrated the cavity FETs show superior high frequency characteristics and high humidity resistance.

STRUCTURE AND FABRICATION

Cavity fabrication process

The cavity structure is a device that forms the space sealed into the surroundings of FETs on a wafer. A fabrication flow of the structure is shown in Figure 1. In (a) an air bridge is formed to cover whole the active area of the GaAs FET. In (b) a polymer repellent thin film is formed

isotropically. In (c) the film is removed by anisotropic dry etching except inside of the air bridge. In (d) a polymer is coated and it is shed by the repellent film. Finally, in (e) a SiN film deposited by p-CVD covers the polymer. Figure 2 shows a photograph of a GaAs FET using this fabrication flow. The polymer is coated only on the active area. This

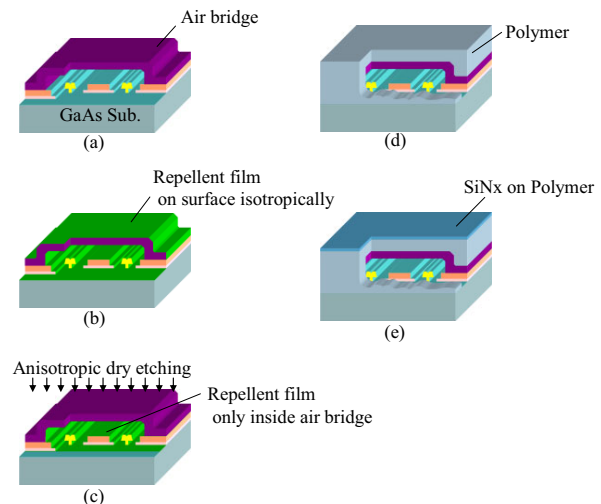


Fig. 1 The fabrication flow of the cavity structure

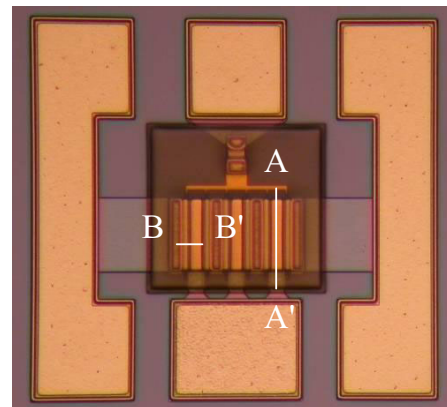


Fig. 2 Photograph of cavity structure FET

fabrication flow is increased by only about 5% or less compared with our conventional structure FET which does not use either polymer or repellent film. So the cost impact of applying this structure is very small.

Repellent film preparation

To form the cavity structure, a high contact angle of the polymers on the repellent films is required. We used self-assembled monolayer (SAM) film of organo-chloro-silane deposited by molecular vapor deposition (MVD) as a repellent film. Figure 3 shows the contact angle of the polymer as a function of the surface conditions. A Si substrate and CFx film on Si were used for comparison with SAM film. The contact angle depends on the kind of surface and the highest value is about 90 degrees on SAM film. This high contact angle helps to form a cavity structure with high reproducibility.

We examined the etching condition of the SAM film, because it should be removed except inside the air bridge. This SAM film can be etched off easily by plasma. We prepared a sample as in Figure 4 to imitate the air bridge shape, and etched the surface by plasma. The space between

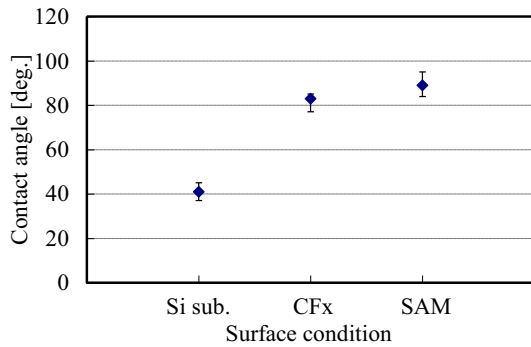
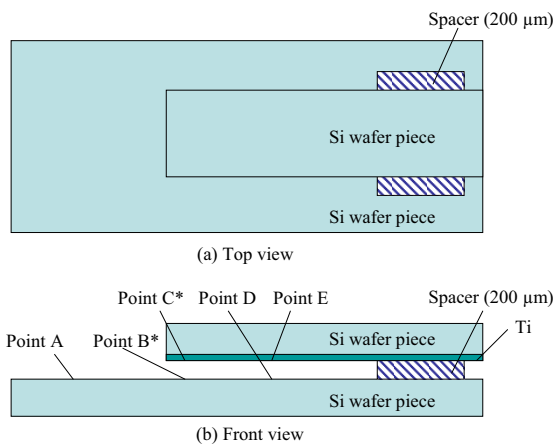


Fig. 3 Contact angle of polymers on Si substrate, CFx film and SAM film.



*Points B and C are several mm away from the end of the upper substrate

Fig. 4 Schematic illustration of test structure to evaluate the etching conditions of SAM film

Table 1 Contact angle of test structure

Plasma Etching Time [sec]	Contact angle of the point in Fig. 4 [degree]				
	A	B	C	D	E
5	<20	60	60	90	90
10	<20	40	40	90	90
20	<20	<20	<20	90	90

the two pieces of Si substrate was 200 μm. Table 1 shows the results of the contact angle of the polymer as a function of the etching time. It was found that the film had been removed from point A because it had a low contact angle of 20 degrees or less at each etching. The contact angle was not decreased at points D and E at any etching time, so the SAM film still remained there. On the other hand, the contact angles of points B and C show the etching time dependence, and were 60 degrees for 5 seconds, 40 degrees for 10 seconds and 20 degrees or less for 20 seconds. This result indicates that the films in these parts are removed depending on the time and it is preferable for etching to be shorter than 5 seconds. However, we selected 5 seconds in consideration of the stability of the plasma.

Evaluation of Cavity structure

We prepared the cavity structure FETs to confirm whether there were differences in the make-up of the structure depending on the plasma etching time of the SAM film. Figures 5a and 5b show cross-sectional SEM images of cavity FETs, with SAM film etched by plasma for 5 and 10 seconds respectively. These are cross-sectional images of A-A' in Figure 2. The polymer has entered the cavity by less than 6 μm from the air bridge edge in Figure 5a, while it is about 20 μm in Figure 5b. This result indicates that the etching condition of 5 seconds is appropriate to fabricate the cavity. Figure 6 shows the B-B' cross-sectional SEM image of cavity FET in Figure 2. It was found that inside of the air bridge has been completely hollowed.

RF CHARACTERISTICS

Figure 7 shows the S-parameters comparison of a

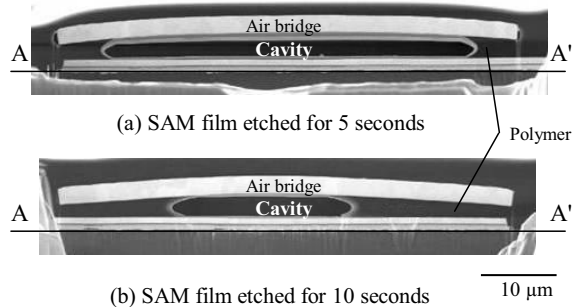


Fig. 5 Cross-sectional SEM image of A-A' in Fig. 2

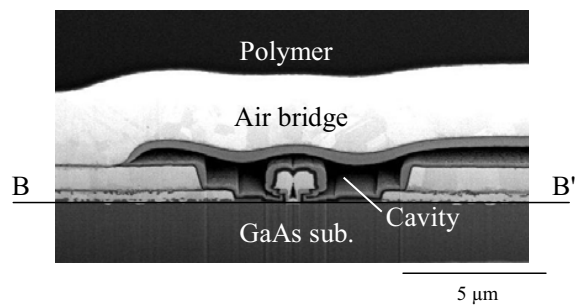


Fig. 6 Cross-sectional SEM image of B-B' in Fig. 2

conventional FET, a cavity FET and a FET filled by polymer inside the air bridge. The cavity FET is very close to the conventional FET and it indicates that the change in capacitance influenced by using the cavity structure is very small, while the difference between the conventional FET and the FET filled by polymer is larger than that of the cavity. Figures 8a and 8b show the MSG @ 10 GHz measured at the 26 points on the wafers of conventional and cavity FETs respectively. Only 0.1 dB of MSG has been decreased and it seems that the influence on the parasitic capacitance is because of the polymer invading about 6 μm into the cavity. Although SAM film remains in the cavity, its parasitic capacitance is enough small to be neglected in the influence on the high frequency characteristics. The standard deviations

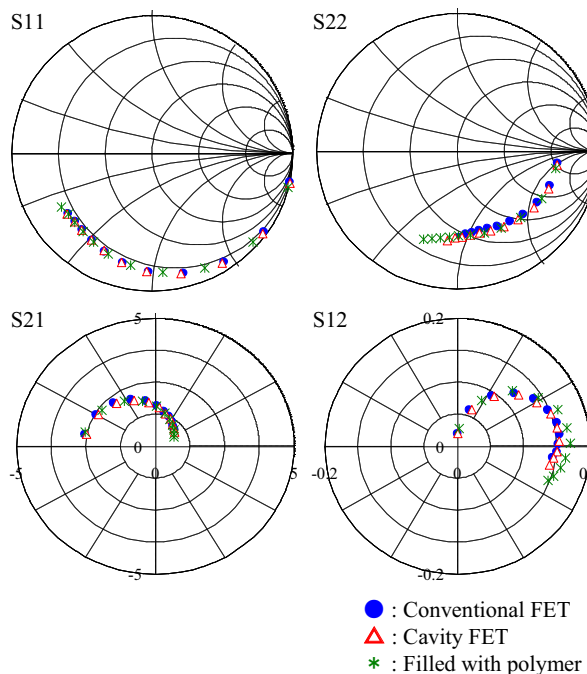


Fig. 7 S-parameters of conventional FET, cavity FET and FET filled by polymer
Frequency is from 1 to 21 GHz in 2 GHz steps

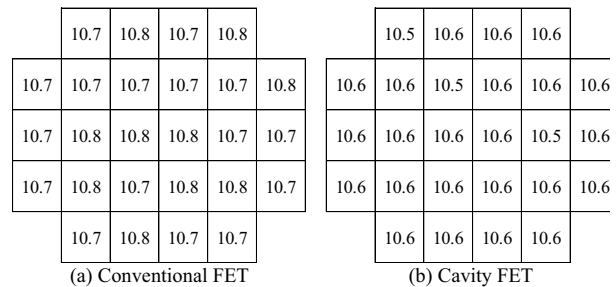


Fig. 8 Wafer map of MSG [dB] measured at 10 GHz

of MSG are 0.023 dB for both conventional and cavity FETs, and the results show that the cavity has been formed very uniformly. If an air bridge is filled with polymer, MSG will decrease by 1 dB or more, so it is understood that the cavity FET is excellent in high frequency characteristics. The gate to source capacitance (C_{gs}) of conventional and cavity FETs are 253 pF and 255 pF respectively, and the gate to drain capacitances (C_{gd}) are 40.2 pF and 41.4 pF respectively.

HUMIDITY

We performed a highly accelerated temperature and humidity stress test (HAST) with bias applied conditions. The HAST was under the conditions of 130°C and 85% RH and biased at $V_{dg} = 11$ V. Table 2 shows the results of the biased HAST. While two-fifths of the samples for the conventional FETs failed within 24 hrs and all samples by 96 hrs, no failure was observed at 96 hrs for the cavity FETs. This result indicates that the humidity resistance is improved

Table 2 Result of biased HAST shown with rejection/number

Test time (hrs)	Conventional FET	Cavity FET
24	2/5	0/5
96	5/5	0/5

greatly by using the cavity structure.

CONCLUSIONS

We conclude that the cavity structure is effective in improving the humidity resistance without degrading the high frequency characteristics and consider it to be the most promising low-cost high frequency device.

ACKNOWLEDGEMENTS

The authors would like to thank Mr. Y. Yokoyama, Mr. Y. Suehiro, Dr. T. Tokunaga, Mr. T. Hisaka, Mr. T. Oku and Dr. N. Yoshida for lots of helpful discussions and for their technical support. Also, the authors would like to acknowledge Mr. K. Nishizawa and Mr. Y. Nishida for sample fabrication and humidity testing.

REFERENCES

- 1) T. Hisaka, H. Sasaki, Y. Nogami, K. Hosogi, N. Yoshida, A. A. Villanueva, J. A. del Alamo, S. Hasegawa, H. Asahi, "Corrosion-induced degradation of GaAs PHEMTs under operation in high humidity conditions", *Microelectronics Reliability* 49 (2009) pp. 1515-1519.
- 2) S. Kumar, J. Kessler, H. Morkner, "6-24 GHz Mixer Using 0.25μm

Enhancement Mode PHEMT Technology in a Low Cost Chip Scale Package", EuMIC 2008, October 2008, pp. 238-241.

- 3) Boris Kobrin, J. Chinn, R. W. Ashurst, "Durable Anti-Stiction Coatings by Molecular Vapor Deposition (MVD)", NSTI-Nanotech 2005, Vol. 2, pp. 347-350.

ACRONYMS

RH: Relative Humidity

DC: Direct Current

HFET: Hetero-junction FET

SiN: Silicon Nitride

p-CVD: Plasma-enhanced Chemical Vapor Deposition

CFx: Fluorocarbon

MVD: Molecular Vapor Deposition

SAM: Self-Assembled Monolayer

HAST: High-Accelerated Temperature and Humidity Stress

MSG: Maximum stable gain

Vdg: Drain to gate voltage