Metal particle effects on thin film capacitors in high volume manufacturing

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Abstract

The effect of metal particles on thin film dielectric capacitors is characterized. Electrical characteristics of statistically significant numbers of capacitors are measured. A figure of merit is derived from the cumulative distribution of capacitor burnout voltages. The figure of merit is correlated with the number of particles per wafer. The use of the figure of merit in establishing process consistency and reproducibility is demonstrated.

OBJECTIVES

The objectives of the present work are:
(1) To use a statistical basis to measure the effect of particles in the lower plate of the capacitor to burnout out voltage of the capacitor.
(2) To derive a statistical figure of merit to rank capacitors on different wafer lots.
(3) To establish the consistency of particle effects on capacitor properties.

INTRODUCTION

Silicon Nitride (Si_3N_4) films are used widely in GaAs integrated circuit manufacturing as the dielectric in metal-insulator-metal (MIM) capacitors. The capacitors occupy a large fraction of the die area in power amplifier and other monolithic microwave integrated circuits (MMICs). One approach to reduce die size (and thereby cost) is to increase the capacitance per unit area of the MIM capacitors by reducing the thickness of the dielectric film. As the dielectric thickness is reduced, it becomes more difficult to maintain the reliability of the capacitor because the effect of particles and other defects becomes more dominant.

In our process, an evaporated gold film forms the lower plate of the capacitor. The gold layer has defects in it such as particles and nodules. The dielectric film is deposited by plasma enhanced chemical vapor deposition (PECVD) from a mixture of SiH_4 and NH_3 at a relatively low temperature (300ºC) which is compatible with GaAs heterojunction bipolar transistor (HBT) device fabrication processes. The low deposition temperature leads to a low-density film as well as high hydrogen content. These process specifics imply that the capacitor "burnout" characteristics could be determined by a combination of both extrinsic and intrinsic defects. The voltage at which the capacitor destructively burns out is called the burnout voltage (Vb). For a dielectric thickness of 0.1µm, we typically measure burnout voltages of approximately 100 V. Defects can reduce the burnout voltages, and in some cases Vb can be zero, a few volts or a few tens of volts. Capacitors with Vb=0 can easily be screened out during functional tests of the circuit. However, capacitors with low Vb are difficult to screen. For this reason, there is a need to quantify the defect level that results in an acceptably small fraction of capacitors with low Vb. Further, the acceptable defect level must be translated into a practical criterion that can be used to certify routinely the quality of capacitors manufactured in high volume.

EXPERIMENTAL APPROACH

In order to statistically measure the effect of particle defects on the capacitor burnout voltage, wafers with different Metal-1 particle counts were created and then all the capacitors were destructively tested. The voltage at which the capacitors burnt out was measured. The differences between wafers with different particle counts were readily apparent when the cumulative distributions (CDs) of burnout voltages were compared.

A statistical figure of merit was derived by noting that the area under the cumulative distribution curve captures the effect of both the number of burnouts as well as the voltage at which burnout occurs. Next, a series of wafers were fabricated under routine conditions over a three-month period in our factory and the applicability of the above techniques to establish process consistency was shown.

Scanning Electron Microscope (SEM) cross-sections of the burnt out regions of capacitors with very low burnout voltages were used to identify the mechanism by which particles affected the burnout voltage.

The new aspects of our work which differ from others in the literature [1,2,3] are the intentional variation of capacitor particles to study their effects, and the proposal of a statistical figure of merit to describe capacitors.

CAPACITOR FABRICATION

A PECVD Silicon Nitride layer deposited between two gold layers forms the MIM capacitor. The lower electrode (Metal-1) is deposited on top of a thin nitride layer, previously deposited on GaAs rendered insulating by ion-implantation. Both the upper and the lower gold films have a thin layer of titanium inserted between the gold and the nitride to promote adhesion. The metal layers are deposited by electron beam evaporation under conditions optimized to result in very low density of particles, “spits” and nodules. A schematic cross-section of the MIM capacitor is shown in Fig.1.

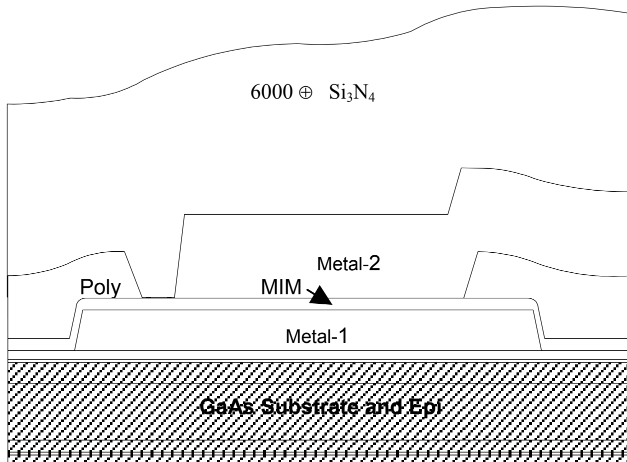

Fig. 1 Cross Section of MIM Capacitor. Metal-1 forms the bottom plate of the capacitor while Metal-2 forms the top plate. Polyimide is used to insulate the Metal-2 from the dielectric layer in non-capacitor areas.

Metal-1 Deposition: A commonly used Ti/Pt/Au metallization is deposited for Metal-1, using electron beam evaporation. The purity of the incoming gold is specified as 99.999%. The gold is deposited from a liner in the crucible and all deposition parameters are optimized for low particle count and nodule formation, while maintaining a reasonable throughput for high volume production.

Dielectric deposition: The MIM nitride is deposited in a Novellus Concept 1 system that is capable of depositing Si_3N_4 films in a plasma generated at low pressures by simultaneous application of low and high frequency electric fields. Although the deposition temperature is only 300ºC, other parameters are optimized for high film density and moderate levels of stress and hydrogen content. The high film density results in a low wet-etch rate of the film. The films inherently have low defects such as pinholes, and excellent conformal coverage because a multiple layer deposition process is used. The films therefore mitigate the effects of sub-micron Metal-1 particles, which thin the nitride film and reduce the local dielectric breakdown field strength.

Metal-2 deposition: Metal-2 is a Ti/Au metal stack deposited in the same manner as Metal-1 on top of the dielectric layer.

CAPACITOR MEASUREMENT

The area of the capacitor under test was 36200 μm^2, and 2886 capacitors per 4" wafer were tested. The voltage across the capacitor plates was varied from 0 to 150 V with a voltage ramp of 25 V/sec from a HP 4156C parameter analyzer. The current was limited to 20 mA. A typical log I versus V curve of a capacitor is shown in Fig 2. The capacitor burnout voltage Vb is defined as the voltage at which the capacitor current shows a step-like increase on a log scale, and reaches the current limit of 20 mA. The capacitor is irreversibly and destructively burnt out at this voltage and current.

EXPERIMENTAL DETAILS

The series of experiments were as follows:

(1) The defect count in Metal-1 was varied keeping the dielectric thickness constant at 0.1 µm to study the effect of Metal-1 defects on capacitors.

The defect count in the Metal-1 was varied to be 6, 178, 632, 1032 and 1654 particles per wafer. The nominal defect count during production is between 6 and 50. Here defects are usually particles, nodules or the result of "spitting" of the melt during deposition. The defect counts were measured on a 100mm blank witness wafer run in the same batch as the product wafer using a Tencor Surfscan 6420. The Tencor system is very sensitive but limited for use on non-patterned wafers. A laser scans the surface of the wafer. The light is reflected into an optical collector and scattered light is assumed to be produced by defects on the surface. The particle counts on the witness wafer and circuit wafer were assumed to be equal.

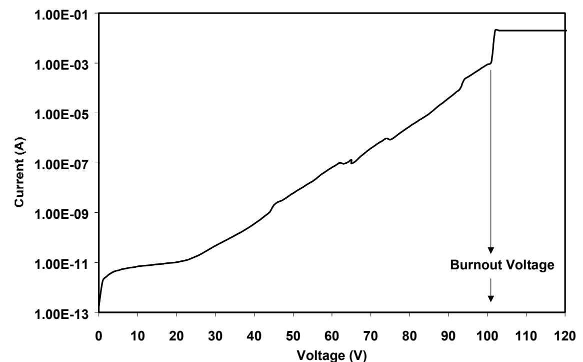

Fig. 2. I/V characteristic of a typical capacitor.

(2) Secondly, 19 wafers with constant dielectric thickness of 0.1 µm were fabricated over a three-month period using two different evaporators under standard production conditions. All capacitors on these wafers were destructively tested to determine the consistency of particle effects on capacitor electrical properties and their figures of merit.

(3) Finally, SEM micrographs of cross sections of the burnt out regions on capacitors with low Vb were obtained.

RESULTS

(1) Cumulative distributions of the burnout voltages for the capacitors in the experiment series (1) above are shown in Fig 3. The burnout voltage of the majority of the capacitors is approximately 100V, as seen from the voltage at which the curve rises steeply. Both the number of capacitors with Vb = 0 (dead shorts) and the number of capacitors with burnout voltages below 100 V increases with increasing particle count. The absolute number of capacitors with Vb=0 is 2, 3, 10, 15 and 30 for the 6, 178, 623, 1032 and 1654 particle count wafers respectively.

Capacitors with Vb <10 V are found only on the 1032 and 1654 particle count wafers.

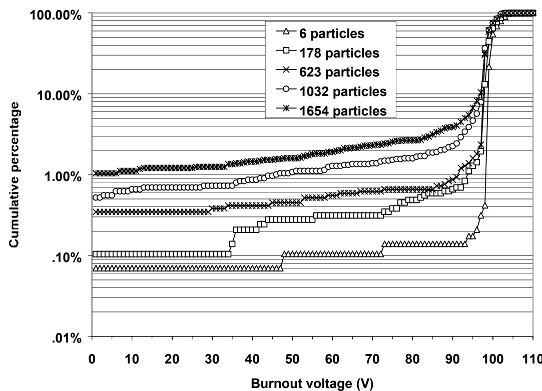

Fig. 3. Cumulative histogram distributions of burnout voltages measured on wafers with different Metal-1 particle counts.

The concept for translating the cumulative distribution into a figure of merit of capacitor quality with respect to Vb is shown schematically in Fig. 4. The characteristic burnout voltage (Vc) is the voltage at which the CD shows a steep increase on a log scale. It is a voltage characteristic of the intrinsic properties of the dielectric and depends mainly on the dielectric thickness. Vc represents the burnout voltage of the majority of the capacitors that were not affected by Metal-1 particles. The figure of merit M is inversely related to the area under the cumulative distribution curve bounded by the Vc and the voltage axis. M is defined as the area times Vc. Multiplication by Vc is physically meaningful because burnout voltage of a sample has to be evaluated relative to the characteristic Vc of the population. Moreover, it results in M being a unitless quantity.

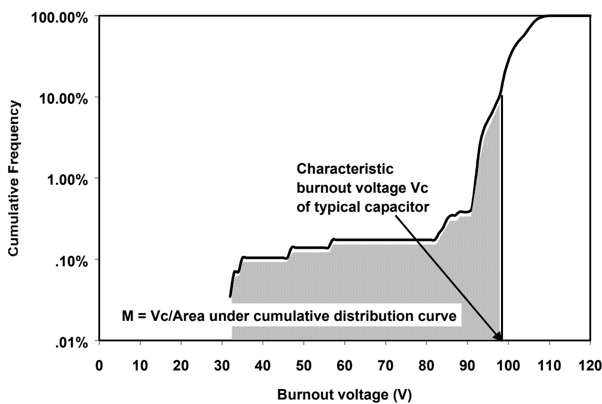

Fig. 4. The figure of merit for the capacitors on the wafer is defined to be Vc/(Area under the cumulative distribution curve). The area is bounded by the distribution curve and the characteristic burnout voltage of the capacitors Vc.

An ideal wafer with no shorted capacitors, with all capacitors having the same burnout voltage Vb and no capacitors with degraded Vb will have M = infinity. A wafer with 100% shorted capacitors will have M = 1.

A plot of M versus number of particles is shown in Fig. 5. M decreases with increasing particle count as expected. Based on (a) the trends seen in the cumulative distributions, (b) the absolute numbers of Metal-1 particles, and (c) the numbers of capacitors with Vb = 0 and low Vb, an acceptable value of M for our application is M = 400. Acceptable M values may be different for other applications.

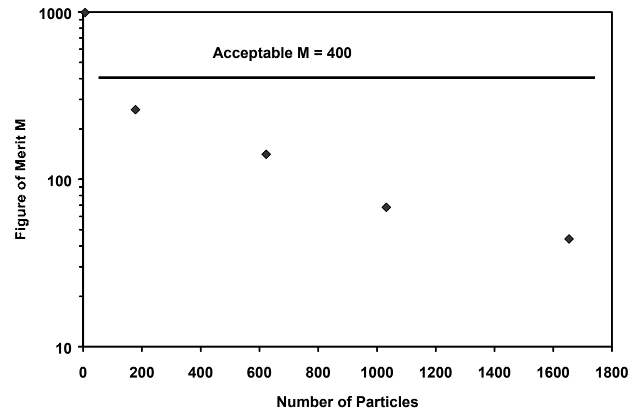

Fig. 5. Figure of merit M for the capacitors on wafers with different Metal-1 particle counts, versus Metal-1 particle count. The acceptable value of M is greater than or equal to 400.

(2) The particle counts on the wafers fabricated from June 10, 2002 to August 27, 2002 are shown in Table I. The high particle count of 612 on June 20 was due to an event in the deposition process that caused spitting in the melt.

TABLE I

Production dates and particle counts of wafers used to check consistency of particle effects.

Date	6-10	6-12	6-18	6-20	6-24	7-22	7-23
Count	60	28	31	612	10	138	1
Date	7-26	7-29	7-31	8-6	8-14	8-16	8-19
Count	0	5	150	49	3	15	6
Date	8-19	8-20	8-21	8-24	8-27		
Count	50	47	0	9	10		

CDs of burnout voltages of capacitors from the first five wafers in the experimental series (3) above are shown in Fig. 6. The CDs of the remaining wafers are similar and are omitted to avoid crowding the graph. The M values were calculated from the CDs as described above. The figure of merit M for each wafer is graphed in Fig. 7. The wafer with 612 particles had a low M value and was below the acceptable M value of 400. The product wafers that were in the same deposition run as the witness wafer with 612 particles were tested with an enhanced electrical screening method at the end of the line to screen out capacitors with

low Vb. The run of 19 wafers and their figures of merit shows that particle effects are consistent and stable with time.

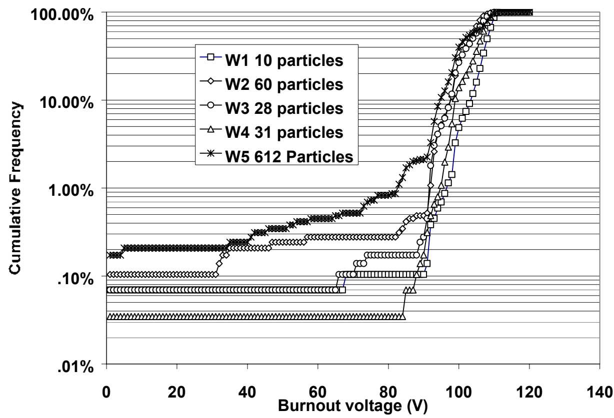

Fig. 6. Cumulative histogram distributions of burnout voltages measured on wafers used for weekly monitoring of Metal-1 particles. The production dates were 6/10/02, 6/12/02, 6/18/02, 6/20/02 and 6/24/02.

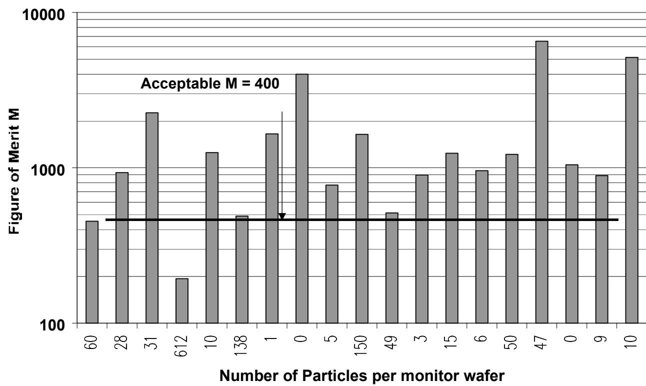

Fig. 7. Figure of merit M for the capacitors on the wafers used for weekly monitoring of Metal-1 particles. The acceptable value of M is 400.

(3) A SEM photograph of a cross section of a capacitor with low Vb is shown in Fig. 8. The cross section is located in the region of the capacitor that burnt out during the electrical test. The Metal-1 particle can be seen. The two plates of the capacitor are fused together at the top of the particle, where the dielectric is thin. The particle causes insufficient photoresist coverage of the dielectric in subsequent etch steps in the process, leading to thinner dielectric at the top of the particle. The higher electric field at the tip of the particle due to thinner dielectric leads to capacitor burn out at the particle. The capacitor burnout mechanism due to Metal-1 particles in our process is due to thinner dielectric at the particle location.

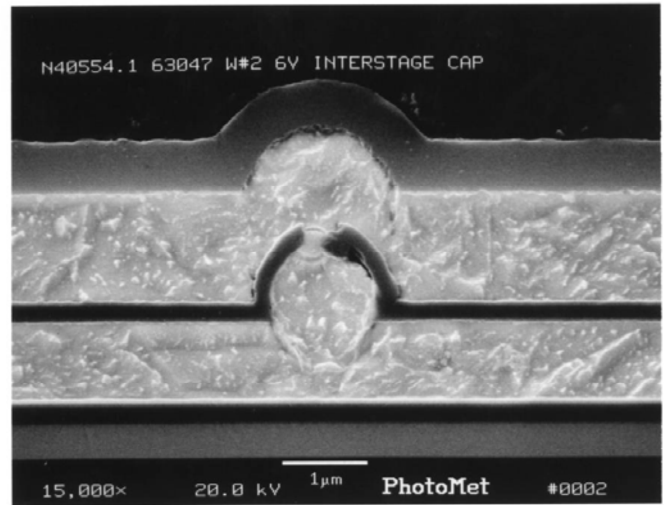

Fig. 8. Scanning electron microscope photograph of a shorted region of a capacitor with a burnout voltage of 6V. The capacitor plates fused through the dielectric at the top of the particle.

CONCLUSIONS

The mechanism of capacitor burnout due to Metal-1 particles in our process is that the capacitor burnout occurs at distinct point-like locations in the capacitor. Hence the capacitor burnout cannot be described by distributed dielectric material parameters. A statistical figure of merit that captures the magnitude of degradation in burnout voltage and the frequency of degradation is required. This work defined and applied such a figure of merit. The characterization of capacitors intentionally created with different Metal-1 particle counts enabled definition of an appropriate lower limit for the use of the figure of merit in production. The consistency of particle effects on capacitor properties was verified by monitoring wafers over a three-month period. Particle effects were consistent and high particle incidents could be detected. The consistency of particle effects on capacitor electrical properties implies that continuous electrical monitoring of capacitors for process control is not necessary for our process. Measurement and control of the particle level in a metal deposition run is necessary and sufficient.

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